WHAT IS CLAIMED IS:

1. An electrically erasable and programmable non-volatile memory cell integrated in a chip of semiconductor material, said memory cell comprising:

a floating gate MOS transistor having a source region and a drain region formed in a first well with a channel defined between the drain region and the source region, a control gate region, and a floating gate extending over the channel and the control gate region; and

a bipolar transistor for injecting an electric charge into the floating gate, the bipolar transistor having an emitter region formed in the first well, a base region consisting of the first well, and a collector region consisting of the channel,

wherein the memory cell includes a second well that is insulated from the first well, and

the control gate region is formed in the second well.

2. The memory cell according to claim 1,

wherein the first well and the second well have a first type of conductivity,

the memory cell further includes a third well having a second type of conductivity, which is opposite the first type of conductivity, and

the first well and the second well are formed in the third well.

3. The memory cell according to claim 2, wherein the floating gate does not extend over the emitter region.

4. The memory cell according to claim 3, wherein a distance between the emitter region and the channel is less than a distance between the emitter region and the source region and less than a distance between the emitter region and the drain region.

5. The memory cell according to claim 1, wherein the floating gate does not extend over the emitter region.

6. The memory cell according to claim 1, wherein a distance between the emitter region and the channel is less than a distance between the emitter region and the source region and less than a distance between the emitter region and the drain region.

7. The memory cell according to claim 6,

wherein at least one of the drain region and the source region has at least one protrusion projecting asymmetrically with respect to a longitudinal axis of the channel, and

the emitter region is arranged at a first side of the longitudinal axis and the at least one protrusion is arranged at an opposite second side of the longitudinal axis.

8. An electrically erasable and programmable non-volatile memory including at least one memory cell, the at least one memory cell comprising:

a floating gate MOS transistor having a source region and a drain region formed in a first well with a channel defined between the drain region and the source region, a control gate region, and a floating gate extending over the channel and the control gate region; and

a bipolar transistor for injecting an electric charge into the floating gate, the bipolar transistor having an emitter region formed in the first well, a base region consisting of the first well, and a collector region consisting of the channel,

wherein the memory cell includes a second well that is insulated from the first well, and

the control gate region is formed in the second well.

9. The memory according to claim 8,

wherein the first well and the second well of the at least one memory cell have a first type of conductivity,

the at least one memory cell further includes a third well having a second type of conductivity, which is opposite the first type of conductivity, and

the first well and the second well are formed in the third well.

10. The memory according to claim 8, wherein the floating gate of the at least one memory cell does not extend over the emitter region.

11. The memory cell according to claim 8, wherein a distance between the emitter region and the channel of the at least one memory cell is less than a distance between the emitter region and the source region and less than a distance between the emitter region and the drain region.

12. The memory according to claim 11,

wherein at least one of the drain region and the source region of the at least one memory cell has at least one protrusion projecting asymmetrically with respect to a longitudinal axis of the channel, and

the emitter region of the at least one memory cell is arranged at a first side of the longitudinal axis and the at least one protrusion is arranged at an opposite second side of the longitudinal axis.

13. The memory according to claim 8, further including means for applying a first voltage to the first well and a second voltage to the control gate region of at least one selected memory cell during an erasure procedure, the first voltage and the second voltage being of opposite signs.

14. An electronic device including an electrically erasable and programmable non-volatile memory and a logic circuit integrated in a chip of semiconductor material, the memory including at least one memory cell that includes:

a floating gate MOS transistor having a source region and a drain region formed in a first well with a channel defined between the drain region and the source region, a control gate region, and a floating gate extending over the channel and the control gate region; and

a bipolar transistor for injecting an electric charge into the floating gate, the bipolar transistor having an emitter region formed in the first well, a base region consisting of the first well, and a collector region consisting of the channel,

wherein the memory cell includes a second well that is insulated from the first well, and

the control gate region is formed in the second well.

15. The electronic device according to claim 14, wherein the memory further includes means for applying a first voltage to the first well and a second voltage to the control gate region of at least one selected memory cell during an erasure procedure, the first voltage and the second voltage being of opposite signs.

16. A method of integrating an electrically erasable and programmable non-volatile memory cell in a chip of semiconductor material, the method including the steps of:

providing a first well;

providing a floating gate MOS transistor having a source region and a drain region formed in a first well with a channel defined between the drain region and the source region, a control gate region, and a floating gate extending over the channel and the control gate region;

providing a bipolar transistor for injecting an electric charge into the floating gate, the bipolar transistor having an emitter region formed in the first well, a base region consisting of the first well, and a collector region consisting of the channel; and

providing a second well insulated from the first well, the control gate region being formed in the second well.

17. The method according to claim 16, further including the step of:

providing a third well having a first type of conductivity,

wherein the first well and the second well have a second type of conductivity, which is opposite the first type of conductivity, and

the first well and the second well are formed in the third well.

18. The method according to claim 16, wherein in the step of providing a floating gate MOS transistor, the floating gate is formed so as to not extend over the emitter region.

19. A method of erasing an electrically erasable and programmable non-volatile memory cell integrated in a chip of semiconductor material, the memory cell including:

a floating gate MOS transistor having a source region and a drain region formed in a first well with a channel defined between the drain region and the source region, a control gate region, and a floating gate extending over the channel and the control gate region, the control gate region being formed in a second well insulated from the first well; and

a bipolar transistor for injecting an electric charge into the floating gate, the bipolar transistor having an emitter region formed in the first well, a base region consisting of the first well, and a collector region consisting of the channel,

the method including the steps of:

applying a first voltage to the first well; and

applying a second voltage to the control gate region so as to provide an erasure voltage between the first well and the control gate region for removing an electric charge from the floating gate, the first voltage and the second voltage being of opposite signs.